Curriculum Vitae

Name: Swagata Saha Sau

Present Position: Head, Assistant Professor, Department of Computer Science, Sammilani Mahavidyalaya, Near Baghajatin Station / E.M. Bypass, Kolkata 700 094.

Previous Position:

1. Lecturer, Department of Computer Science & Engg., BIT, Kolkata

2. Guest Lecturer in Dept. of Instrumentation & Electronics, Jadavpur University.

Educational Qualification:

Name of the Examination	University / board	Year of passing	Subject	Division /Class
Ph. D.	University of Calcutta	Pursuing	Wire Length Minimization in Multi-Layer Channel Routing for VLSI Circuit Synthesis	
M.Tech.	ISM, Dhanbad	2003	Computer Application	I First (Gold Medalist)
B.Ed.	Calcutta University	1997	General	I
M.Sc.	IIT, Kharagpur	1996	Mathematics. C Lang., Data structure, DBMS, OS, Complier etc	I
B.Sc.	Calcutta University	1993	Math (Hons), Phy (P), Chem (P)	II
Higher Secondary	WBCHSE	1990	Mathematics, Physics, Chem, Biology, Bengali, English	I
MP (Class X)	WBBSE	1988	General	I

Other Qualifications:

GATE:

Qualified GATE Exam in the year 2001 with **95.39** percentile (All India Rank: 0039)

NET:

Qualified joint CSIR-UGC Junior Research Fellowship (JRF) and Eligibility for Lectureship – National Eligibility Test (NET) held on 30.12.2001

Teaching experience: More than 20 years

For B.Sc.:

i) Project work on VLSI Physical Design, Image Processing, Artificial Intelligence etc. ii) Programming Languages (C, C++ etc) iii) Computer Graphics iv) Formal language and Automata theory/ Theory of Computation v) Operational Research and Optimization Techniques vi) Data Structures vii) DBMS viii) Operating System ix) Digital Image Processing x) Computational Intelligence xi) Design and analysis of Algorithm

For B.Tech & MCA/M. Sc.:

i) Artificial Intelligence ii) Programming Languages (C, C++ etc) iii) Image processing iv) Formal language and Automata theory v) Operational Research and Optimization Techniques vi) Data Structure vii) DBMS viii) Operating System ix) Design & Analysis of Algorithm x) Computer Graphics xi) Project

For M.Tech.:

Acted as Guest Supervisor for conducting final year M.Tech. Project in the University of Calcutta and University of Technology, Kolkata.

Seminar and Conference Attend:

i) "Computer Applications for the 21st Century- Synergies & Vistas", UGC-DST-CFSL sponsored two day National Conference organized by Department of Computer Science, Vidyasagar College, W.B., Dec. 11-12, 2008.

ii) TEQIP sponsored One day Seminar on "Soft Computing & Bio-Informatics Applications" organized by Department of Information Technology & CSE, Kalyani Govt. Engg. College, W.B., April 30, 2008.

iii) "International Conference on Distributed Computing & Networking (ICDCN 2010)" organized by University of Calcutta during January 3-6, 2010.

iv) "International Conference on Computing and Systems (ICCS-2010), November 19-20, 2010.

v) 24th VLSI Design Conference and 10th international conference on Embedded Systems, 1st January 2011 - 8th January 2011.

vi) 3rd International Conference on "Recent Advances in Mathematics, Technology and Management", BITM, Santiniketan, WB, India, Mar. 19-20. 2011.

vii) 2011 IEEE International Conference on Computer Science and Automation Engineering (CSAE 2011), Shanghai, China, June 10-12. 2011.

viii) 5th International Conference on Computers and Devices for Communication (CODEC 2012), Kolkata, December 18-20, 2012.

ix) 1st International Doctoral Symposium on Applied Computation and Security Systems (ACSS 2014), Kolkata, April 18-20, 2014.

x) 17th International Symposium on VLSI Design and Test, VDAT – 2013, Kolkata, July 2013.

xi) 18th International Symposium on VLSI Design and Test, VDAT – 2014, Coimbatore, 16th- 18th, July 2014.

xii) 29th VLSI Design Conference and 15th international conference on Embedded Systems, 4th January 2011 - 8th January 2016.

xiii) National Seminar on Applications of Distributed Systems Recent Trends, Kolkata, 4th March 2016.

Course Attend:

i) "A Concise Course on the Design and Analysis of VLSI Circuits" organized by Department of Electronics and Telecommunication Engineering, Jadavpur University during December 13-17, 2005.

ii) UGC Sponsored Refresher Course on "Computer Applications" organized by University of Kalyani, W.B, January 8-28, 2008.

iii) UGC Sponsored Orientation Programme organized by UGC-Academic Staff College, Jadavpur University, Kolkata during November 17th – December 15th, 2008.

iv) UGC-NRCPS Sponsored Summer School on Techniques for Design, Fabrication and Computation of Integrated Circuits (TECHNOMICS - 12), organized by Institute of Radio Physics and Electronics, University of Calcutta, May 23rd – June 13th, 2012.

And many more.

Paper Publication:

List of Publication in the Field of VLSI Physical Design

[1] Pal A., A. K. Khan, S. Saha Sau, A. K. Datta, R. K. Pal, and A. Chaudhuri, Application of Graphs in Computing Reduced Area VLSI Channel Routing Solutions, *Proc. of International Conference on Computing and Systems* (*ICCS-2010*), pp. 249-256, 2010.

[2] Pal A., T. N. Mandal, S. Saha Sau, A. K. Datta, R. K. Pal, and A. Chaudhuri, Graphs – The Tool to visualize The Problems in VLSI Channel Routing, *Assam University Journal of Science and Technology; Physical Sciences and Technolgy,* vol – 7, No. – II, pp. 73-83, 2011.

[3] Pal A., S. Saha Sau, T. N. Mandal, A. K. Datta, R. K. Pal, and A. Chaudhuri, An Efficient Heuristic to Find Reduced Area VLSI Channel Routing Solutions with Floating Terminals, *Assam University Journal of Science and Technology; Physical Sciences and Technolgy,* vol – 8, 2011.

[4] Saha Sau S., A. Pal, T. N. Mandal, A. K. Datta, R. K. Pal, and A. Chaudhuri, A Graph based Reduced Area VLSI Channel Routing Algorithm with Floating Terminals, *International Journal BITM Transactions on EECC, ISSN No.-0974-9527,* vol - 2, No. -1, pp. 83-93, 2010.

[5] Saha Sau S., A. Pal, T. N. Mandal, A. K. Datta, R. K. Pal, and A. Chaudhuri, A Graph based Algorithm to Minimize Total Wire Length in VLSI Channel Routing, *Proc. of 2011 IEEE International Conference on Computer Science and Automation Engineering* (*CSAE 2011*), vol – 3, pp. 61-65, 2011.

[6] Pal A., S. Saha Sau, T. N. Mandal, A. K. Datta, R. K. Pal, and A. Chaudhuri, Yet An Efficient Algorithm for Computing Reduced Area VLSI Channel Routing Solutions with Floating Terminals, *Proc. of International Conference on ICCIT - 2011,* 2011.

[7] Saha Sau S., R. K. Pal, An Efficient High Performance Parallel Algorithm to Yield Reduced Wire Length VLSI Circuits, *Proc. of* 5th *International Conference on Computers and Devices for Communication* (*CODEC 2012*), p.n. -1-4, DOI: 10.1109/CODEC.2012.6509278, 17-19 Dec. 2012.

[8] Saha Sau S., R. K. Pal, An Efficient Algorithm for Reducing Wire Length in Three-Layer Channel Routing, , *Applied Computation and Security Systems*, vol - 2, Part III, pp 145-156, 978-81-322-1987-3 in Series Advances in Intelligent Systems and Computing, Vol. 305, Rituparna Chaki et al. (Eds) Volume 305, 2015, Print ISBN: 978-81-322-1987-3, Online ISBN: 978-81-322-1988-0, 27 Aug 2014, DOI: 10.1007/978-81-322-1988-0_9, Publisher: Springer India.

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[9] Saha Sau S., R. K. Pal, A Re-router for Optimizing Wire Length in Two and Four-Layer No-Dogleg Channel Routing, *Proc. of 18th International Symposium on VLSI Design And Test*, VDAT – 2014, p.n.-1-6, DOI: 10.1109/ISVDAT.2014.6881057, Publisher: IEEE 978-1-4799-4006-6/14/2014 IEEE, 16th- 18th, July 2014.

[10] Saha Sau S., R. K. Pal, A Re-router for Reducing Wire Length in Multi-layer No-dogleg Channel Routing, *International Journal of Computer Trends and Technology* (*IJCTT*), Volume 38, Number 2, p.n. – 110-118, August 2016.

List of Publication in the Field of Image Processing

[1] Saha S., P. K. Jana, "A Parallel Algorithm for Medial Axis Transformation", *Proc. of the 2003 International Symposium of Parallel and Distributed Processing and Application*, LNCS 2745, pp. 356-361, 2003, Springer-Verlag Berlin Heidelberg 2003.

Chair Person of the Conference :
2011 IEEE International Conference on Computer Science and Automation Engineering (CSAE 2011), Shanghai, China, June 10-12. 2011: Session D2 & D4.

Research Work: Doing research work (Ph.D.) in the Department of Computer Science and Engineering, University of Calcutta in the field of VLSI Physical Design.

Topic of Ph. D. Thesis: "Wire Length Minimization in Multi-Layer Channel Routing for VLSI Circuit Synthesis"

Awards, fellowships etc. received:

[1] Awarded Gold Medal in M. Tech, 2003.

[2] Awarded the fellowship to attend 24th International Conference for VLSI Design and 10th International Conference for Embedded Systems, Chennai, Jan 2th - Jan 7th 2011.

[3] Awarded Teacher Fellowship under Faculty Development Programme sanctioned by the University Grants Commission (Sanction Letter No. F.TF.WC-003-01/12-13 (ERO) dated 10.05.2012.

[4] Awarded the fellowship to attend 26th International Conference for VLSI Design and 12th International Conference for Embedded Systems, Pune, Jan 5th - Jan 9th 2013.

[5] Awarded the fellowship to attend 18th International Symposium on VLSI Design And Test, VDAT – 2014, Coimbatore, 16th- 18th, July 2014 VDAT-2014.

[6] Awarded the fellowship to attend 29th International Conference for VLSI Design and 15th International Conference for Embedded Systems, Kolkata, Jan 4th - Jan 8th 2016.

Membership International / National / State Committees

[1] Member of **IEEE**. **Membership No. 92358798 (2014).**

[2] Member of **UG board of studies**, Computer Science, University of Calcutta since 2008.